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Improved single-phase PLL structure with DC-SOGI block on FPGA board implementation

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Abstract - **Synchronization block which is used as a part of photovoltaic (PV) inverters control structure has a key impact on connecting inverters with grid. One of the most important parameters in the point of connection PV inverter and grid is phase angle between grid voltage and inverter current. This angle determines the energy transfer between inverter and grid. Synchronization algorithms have developed for very long time. At first, they were based on zero crossing grid voltage detection, while today complexed synchronization algorithms implemented on high performance digital board have been used. One of these synchronization structures is Phase Locked Loop – PLL. In this paper implementation of improved PLL structure is presented. This improved structure is special while it has possibility of grid parameters estimation even if grid voltage has noise or DC offset. This DC offset from the grid in PLL structure usually entered via measurement and A/D conversion processor or may be generated due to temporary system faults. Appearance of DC offset in measured grid voltage on the one hand prevents any estimation process of grid parameters and on the other hand also degrades reference sine signal at the output of PLL structure in PV inverters. This improved structure is designed in digital form and implemented on FPGA digital board and experimental results of this implementation are presented. Obtained experimental results show that the proposed PLL structure successfully solves important issue such is presence of DC offset in measured grid voltage.**

Keywords - SRF-PLL; two-phase generator; DC-SOGI block; DC-offset; FPGA implementation.

I. INTRODUCTION

Synchronization block is necessary part of a control structure when PV inverters connect with grid, and it is used to adjust phase angle between grid voltage and inverter current. One of the most widely used synchronization structures is Phase Locked Loop – PLL. In this paper is analyzed implementation of Synchronous Reference Frame Phase Locked Loop – SRF-PLL structure with DC-SOGI (Second Order Generalized Integrator with DC offset elimination) used for PV inverter synchronization, on FPGA board. This improved PLL structure is presented in [1], and is specific while DC-SOGI block which is phase detector has possibility of DC offset and noise elimination, so the whole structure can estimate grid parameters even if the grid voltage is contaminated by noise or harmonics.

Thanks to its simple realization, robustness and efficiency, SRF-PLL is probably the most popular structure for obtaining information on grid voltage parameters. In Fig. 1 is shown a block diagram of this single-phase PLL structure. The SRF block works as a phase detector, which transforms stationary voltage components (αβ) into DC components (dq) of the synchronous reference system using Park transformation. This block is adaptive by the estimated phase angle, therefore output of PLL structure has such impact on amplitudes of the vectors v_d and v_q, so that the signal v_q is reduced to zero. At the same time, the value of v_d converges to the amplitude of the grid voltage. The PI controller is used as a loop filter. In addition, in order to make the SRF-PLL structure robust to grid amplitude changes, the signal v_q is divided by the estimated amplitude of the grid signal, which can be obtained by filtering the v_d signal using the low pass filter.

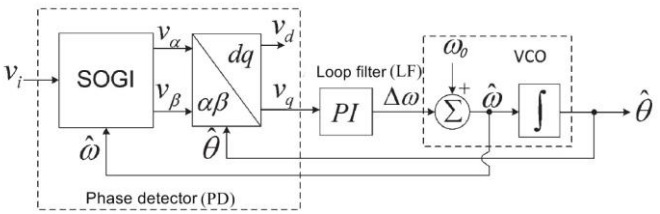

Figure 1. SOGI-PLL structure

This structure is very popular at three-phase systems due to its efficiency and simplicity. However, in the case of single-phase systems, due to the lack of independent input signals, such as in three-phase systems, its application is more complicated.

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Therefore, some methods are proposed for generating an orthogonal signal using input signal in the single phase system so the application of the Phase Detector (PD) block is possible.

In the literature, a large number of different PD blocks are known, but actualy their realization is based on SOGI and inverse Park OSG blocks, so these structures are also called SOGI PLL and Park PLL structure [2-4]. They have acceptable performances even under conditions of varying frequency of grid voltage or in the presence of harmonics and noise, which are the most common input signal disturbances. However, if the input signal has a DC offset or an asymmetry, the phase difference at the output of the two-phase generator is not exactly $\pi/2$, so an error in the estimation of grid parameters will occur. In [1] is detaily described a DC-SOGI block that has the possibility to eliminate a DC offset or noise if they exist at the input of SRF-PLL structure. Modifying a two-phase generator, adding a control loop to the generator itself, generation of quadrature signals and elimination of DC offset without the addition of any filters is enabled. The proposed generator is robust and has a fast response to changes in grid parameters. It also effectively eliminates noise in the measured grid voltage.

II. DC-SOGI BLOCK

As it is already mentioned, DC-SOGI block is a part of the SRF-PLL structure. The phase detector in the SRF-PLL structure [1-4] is the SRF block (*αβ/dq* block - Fig. 2 a). At the input of the SRF block, it is necessary to have two signals phase shifted by $\pi/2$, $v_\alpha(t)$ and $v_\beta(t)$, which are the output signals of the SOGI block. The SOGI block consists of two second-order filters, $W_\alpha(s)$ which is bandpass filter and the low-pass filter $W_\beta(s)$, so that both can effectively supress high-frequency noise, but not a DC offset if it appears in the measured grid signal. The tranfer functions of these filters in a continious domain are given by equations (1) and (2).

$$W_\alpha(s) = \frac{\omega s}{s^2 + \omega s + \omega^2} \tag{1}$$

$$W_\beta(s) = \frac{\omega^2}{s^2 + \omega s + \omega^2} \tag{2}$$

For the operation of a two-phase generator, it is also important, that estimated frequency ω_{est} is same as frequency ω, which means it should be frequency-adaptive. DC offset causes unwanted waves in the grid frequency and amplitude estimated values at the output of the PLL structure. Therefore, it was necessary to make some changes to the existing SOGI block. This enhanced SOGI block is called DC-SOGI. A block diagram of the SRF-PLL structure with a DC-SOGI block and a block diagram of the DC-SOGI block itself are shown in Fig. 2 a) and Fig. 2 b).

Transfer function of DC-SOGI block is given by the following equations:

$$W_{m\alpha}(s) = \frac{V_\alpha(s)}{V_g(s)} = \frac{\omega s^2}{s^3 + (\omega + k_i)s^2 + \omega^2 s + k_i\omega^2} \tag{3}$$

$$W_{m\beta}(s) = \frac{V_\beta(s)}{V_g(s)} = \frac{\omega^2 s}{s^3 + (\omega + k_i)s^2 + \omega^2 s + k_i\omega^2} \tag{4}$$

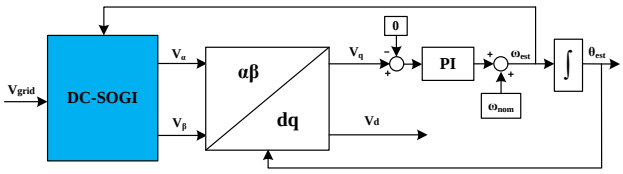

Figure 2a. Block diagram of single-phase SRF-PLL structure

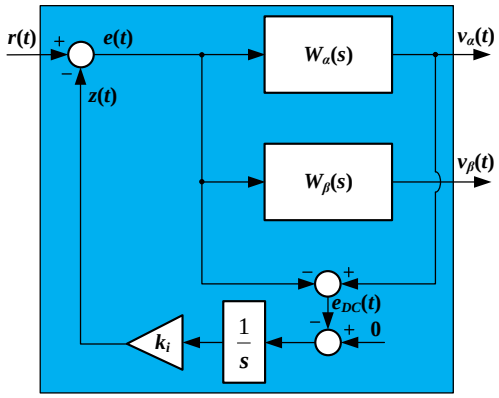

Figure 2b. Block diagram of DC-SOGI block

Filters of the DC-SOGI block $W_{m\alpha}(s)$ and $W_{m\beta}(s)$ can eliminate the DC offset while the SOGI block is not able to. If it is assumed that the measured grid voltage $r(t)$ contains DC offset, the value of this DC offset is estimated at the control loop output and then subtracted from the input voltage superimposed with DC offset. The key parameter of proposed closed loop is the integral gain k_i .

Both and $W_{m\beta}(s)$ filters are band-pass filters and have identical denominators, but different nominators. Filter $W_{m\alpha}(s)$ in numerator has ωs^2, and the filter $W_{m\beta}(s)$ has $\omega^2 s$. This difference in numerators is essential for generating two signals $v_\alpha(t)$ and $v_\beta(t)$ phase-shifted for $\pi/2$ at the output of DC-SOGI block. If s is replaced with $j\omega$ in (3) and (4), it can be concluded that the $W_{m\alpha}(s)$ filter introduces a zero phase delay, while the $W_{m\beta}(s)$ filter introduces a phase delay of $\pi/2$ regarding measured grid voltage $r(t)$. Frequency band-pass filters do not pass DC offset and high-frequency noise if the input voltage contains them at all.

III. DC-SOGI BLOCK RESPONSE

If it is assumed that the measured grid voltage contains a DC offset it can be expressed as: $v_{in}(t) = V_{in}\cos(\omega t) + C$, where $v_{in0}(t) = V_{in}\sin(\omega t)$ is sinusoidal signal without DC offset, while C is DC offset. Laplace transformation of v_α and v_β signals at output of two-phase generator is given by:

$$V_\alpha(s) = W_{m\alpha}(s)V_{in0}(s) + W_{m\alpha}(s)\frac{C}{s} \tag{5}$$

$$V_\beta(s) = W_{m\beta}(s)V_{in0}(s) + W_{m\beta}(s)\frac{C}{s} \tag{6}$$

After performing the inverse Laplace transform, the equations (5) and (6) show that the signals v_α and v_β are:

$$v_\alpha(t) = V_{in}\cos(\omega t) - A_1 e^{-t/\tau_1} - A_2 e^{-t/\tau_2}\cos(\omega_1 t) + \\ + A_3 e^{-t/\tau_2}\sin(\omega_1 t) \tag{7}$$

$$v_\beta(t) = V_{in}\sin(\omega t) + A_4 e^{-t/\tau_1} - A_5 e^{-t/\tau_2}\cos(\omega_1 t) - \\ - A_6 e^{-t/\tau_2}\sin(\omega_1 t) \tag{8}$$

It is obvious that the exponential components in equations (7) and (8) disappear after (3-5) τ_1 and τ_2, so the signals $v_\alpha(t) = V_{in}\cos(\omega t)$ and $v_\beta(t) = V_{in}\sin(\omega t)$ at output of two phase generator are phase shifted for $\pi/2$. From (3) and (4) it is clear that the value of the integral gain k_i determines the pole position of the functions $W_{m\alpha}(s)$ and $W_{m\beta}(s)$ in s-plane, so the parameter k_i determines the values of the time constants τ_1 and τ_2, amplitude A_i, i=1, 2, ..., 6, and frequency ω_1 in the time domain, which affects the response of the two-phase generator during the transition process. If the real and conjugated complex roots of the characteristic polynomial $D(s)$ are $-a$ (a> 0) and $-\xi\omega_n \pm \underbrace{j\omega_n\sqrt{1-\xi^2}}_{\omega_1} = -\xi\omega_n \pm j\omega_1$, respectively, where ζ (0<ζ<1) is damping factor, and ω_n is natural frequency, then:

$$s^3 + (\omega + k_i)s^2 + \omega^2 s + k_i\omega^2 = (s+a)(s^2 + 2\xi\omega_n s + \omega_n^2) \\ = s^3 + (a + 2\xi\omega_n)s^2 + (\omega_n^2 + 2\xi\omega_n a)s + a\omega_n^2 \tag{9}$$

From (9):

$$\omega + k_i = a + 2\xi\omega_n \tag{10}$$

$$\omega^2 = \omega_n^2 + 2\xi\omega_n a \tag{11}$$

$$k_i\omega^2 = a\omega_n^2 \tag{12}$$

Terms for a, ζ and ω_n depend on parameter k_i are given by equations (10)-(12). Therefore, time constants $\tau_1 = 1/a$, $\tau_2 = 1/\zeta\omega_n$ and frequency ω_1 from (7) and (8) can be determined using k_i parameter. Optimal value of k_i can be determined from conditions of the equality of real root ($-a$) and real part of conjugated-complex root ($-\zeta\omega_n$). Using $a = \zeta\omega_n$ in (10)-(12) is obtained:

$$\omega + k_i = 3a \tag{13}$$

$$\omega^2(a - k_i) = 2a^3 \tag{14}$$

Using $\omega = 2\pi f$, f=50 Hz (grid frequency) and solving (13) and (14) for a and k_i is obtained:

$$a = 133.1576 \tag{15}$$

$$k_i = 85.3135 = k_{iopt} \tag{16}$$

The obtained value of parameter k_i from (16) is optimal.

IV. DC-SOGI BLOCK IN DISCRETE DOMAIN

Digital devices such as FPGA, Digital Signal Processor (DSP), etc. are commonly used for signal processing. In order to implement a control structure on a digital device, such as PLL, it is necessary to discretize the structure first, which implies discretization of each individual block of the structure. During the discretization process, it is necessary to chose sample time, which significantly influences the operation of the DC-SOGI block. In [5] is analyzed the stability, the response of the DC-SOGI block and the entire SRF-PLL structure.

As already mentioned, one of the key components of the single-phase SRF-PLL structure is a two-phase generator that generates two phase-shifted signals $v_\alpha(t)$ and $v_\beta(t)$ from the single-phase measured grid voltage. The two-phase generator is made of two second order filters.

Applying bilinear transformation on transfer functions (1) and (2) transfer functions of these filters in z-domain are gained:

$$W_\alpha(z) = r\frac{z^2 - 1}{z^2 + pz + q} \tag{17}$$

$$W_\beta(z) = t\frac{z^2 + 2z + 1}{z^2 + pz + q} \tag{18}$$

where:

$$r = \frac{a}{a+b+4},\ t = \frac{b}{a+b+4},\ p = \frac{2(b-4)}{a+b+4},\ q = \frac{b-a+4}{a+b+4},$$
$$a = 2\omega T_s,\ b = (\omega T_s)^2$$

The bilinear transformation maps the s- plain left half to the interior of the unit circle in the z-domain, which means that if a transfer function is stable in the s-domain, its image in the z-domain is also stable. Regardless of this, a rigorous proof of the filter transfer functions in the z-domain stability was performed [5]. The $W_\beta(s)$ filter is a low pass filter and it can not eliminate the DC offset if it occurs in the measured grid voltage. Thus, in general, the two-phase generator itself can not eliminate the induced DC offset unless the loop proposed in [5] is applied. The block diagram of the DC-SOGI block in the z-domain is shown in Fig 3.

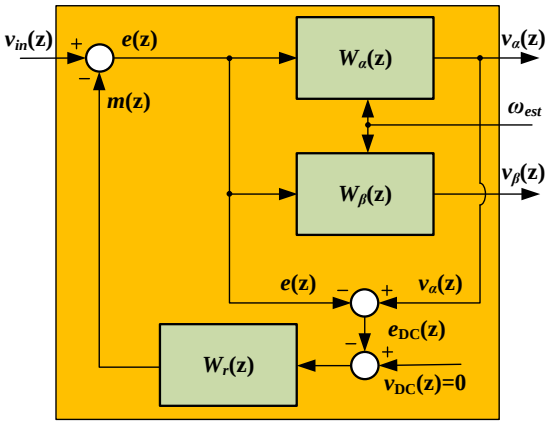

Figure 3. Block diagram of discrete DC-SOGI block [5]

From block diagram at Fig. 3 it is clear that discrete blocks perform the same function as those in the continious domain. Thus, if the discrete input grid voltage $v_{in}(z)$ contains a DC-offset, $W_\alpha(z)$ acts as a frequency band-pass filter, so it does not pass through a DC component, and the estimated value of the DC offset $e_{DC}(z)$ is difference between signals at the input and output of this filter: $e_{DC}(z) = e(z)–v_\alpha(z)$. The DC offset is further compared to its reference value $v_{DC}(z)=0$ and the error is passed through the simple regulator (integrator) $W_r(z)$, and substracted from the input signal that contains DC offset. This way, the DC offset that existed in the measured input signal $v_{in}(z)$ will be eliminated. As already mentioned, the key parameter of the DC-SOGI block control loop, for DC offset elimination, is a parameter that determines the dynamics of the DC offset elimination. Transfer functions of the modified filters $W_{m\alpha}(z)$ and $W_{m\beta}(z)$, according to Fig. 3, are:

$$W_{m\alpha}(z)=\frac{V_\alpha(z)}{V_{in}(z)}=\frac{W_\alpha(z)}{1+W_r(z)\left[1-W_\alpha(z)\right]} \tag{19}$$

$$W_{m\beta}(z)=\frac{V_\beta(z)}{V_{in}(z)}=\frac{W_\beta(z)}{1+W_r(z)\left[1-W_\alpha(z)\right]} \tag{20}$$

Used DC-SOGI control loop controller is a simple integrator and in z-domain using a bilinear transformation its transfer function is:

$$W_r(z)=k_i\frac{T_s}{2}\frac{z+1}{z-1},\ G_r(z)=k_i^*\frac{z+1}{z-1},\ k_i^*=k_i\frac{T_s}{2} \tag{21}$$

After arranging and simplifying $W_{m\alpha}(z)$ and $W_{m\beta}(z)$ can be written as:

$$W_{\alpha m}(z)=\frac{r\left(z^3-z^2-z+1\right)}{z^3+p_1z^2+p_2z+p_3} \tag{22}$$

$$W_{\beta m}(z)=\frac{t\left(z^3+z^2-z-1\right)}{z^3+p_1z^2+p_2z+p_3} \tag{23}$$

where:

$$p_1=\frac{p+k_i^*(1-r+p)-1}{1+k_i^*(1-r)},\ p_2=\frac{q-p+k_i^*(r+p+q)}{1+k_i^*(1-r)},$$
$$p_3=\frac{k_i^*(r+q)-q}{1+k_i^*(1-r)},$$

It is clear that both modified DC-SOGI block filters $W_{m\alpha}(z)$ and $W_{m\beta}(z)$ are band-pass filters and do not pass either a DC component or a high-frequency noise if they occur in the measured grid voltage. Proposed filter does not pass DC component and it is confirmed using the limit value theorem in z-domain.

The next step is to determine the impact of the integral gain k_i on the estimation parameters and DC component elimination at the output of a two-phase generator. The appereance of a DC offset at the input of a two-phase generator can be viewed as step change, so it is interesting to observe the response of the two-phase generator precisely to this disorder. From the theory of discrete systems it is known that the conjugate complex roots of the characteristic polynomial $D(z)$ closest to the boundary of the unit circle in z-domain, have a dominant influence on the character of the discrete system transient process. In this case, a pair of conjugated complex roots $z_{2,3}=\sigma_z\pm j\omega_z$ have a key imact on the transition process. Conjugated complex roots can be written as:

$$z_{2,3}=r\left|\pm\theta,\ r=\sqrt{\sigma_2^2+\omega_z^2},\ \theta=arctg\frac{\omega_z}{\sigma_2}\right. \tag{24}$$

Dominant time constant T_d of transition process regarding this conjugated complex roots is given as: $T_d=-\frac{T_s}{\ln r}$. In this case for $(4\div6)T_d$ the constant is T_d =0.0075 s. That means that transition proces ends in $(4\div6)T_d$ which is about 0.045 s.

DC offset estimation time at the output of control loop ($W_r(z)$ - Fig. 3) is shown in Fig. 4 for three different values od parameter k_i and for two limit values of DC offset in measured signal: 2%@230 V and 50%@230 V.

For small values of parameter k_i (k_i=10), DC offset estimation time at control loop output is about 0.5s, which is very longime. In the other hand if the parametar value is big k_i (k_i=500) unwanted oscilation occure, and last about 0.3s, which is not good too. For optimal value of parameter k_i ($k_i = k_{opt}$=85.64) transition process end in 0.05s which is accordant with previous analysis.

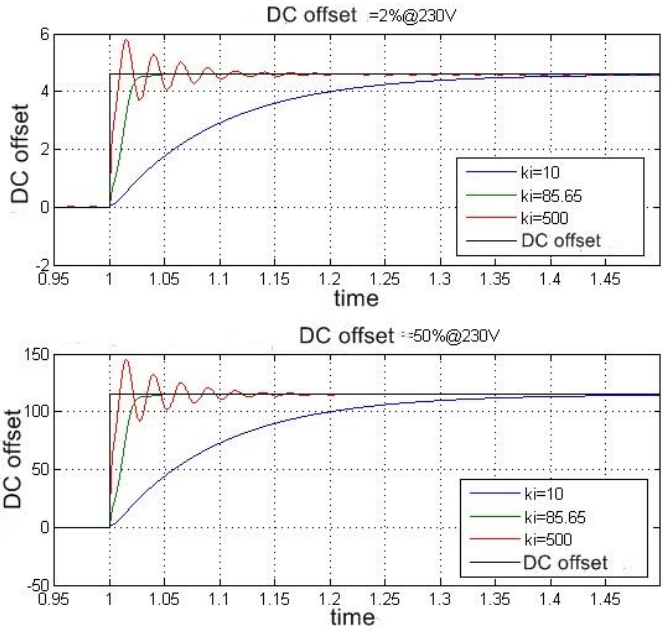

Figure 4. DC offset estimation time at output of control loop for three different values of parameter k_i and for two different values of DC offset 2%@230 V and 50%@230 V

V. RESULTS OF EXPERIMENT

Structures and algorithms for signal filtering are mostly implemented on digital hardware. As the digital hardware in this work, the FPGA board was used. FPGA belongs to a type of programmable circuit where different digital structures

(control structures/algorithms) can be realized and which can be programmed/reprogrammed outside the production. Modern FPGA boards can contain elements such as processor cores, PLL circuits, embedded RAM memory, etc. Programming languages that are used for programming FPGA are called Hardware description languages (HDL), most common are the VHDL (VHSIC - Hardware High Speed Integrated Circuit) and Verilog (standardized IEEE 1364 programming language). In addition to writing in the HDL editor, the codes in these programming languages can be automatically generated from other programs, such as MATLAB, Quartus, and so on. Generation of HDL code in the MATLAB environment is possible from: Simulink model, Stateflow diagrams, Embedded MATLAB blocks and tools for creating digital filters. The technique for HDL code generation from the MATLAB environment is described in detail in [6]. Already designed, improved SRF-PLL structure in Simulink was matched to the MATLAB HDL encoder, and then the obtained HDL codes were verified in the ModelSim program, and then used for programming the FPGA circuit. The results obtained by the simulations in MATLAB/Simulink and ModelSim environment are compared to those obtained in experiments.

Used FPGA is located on the Altera DE2 board from the Cyclone II family [7]. In order to observe the signals from the DE2 board on an oscilloscope and record it, it was necessary to perform a digital to analogue conversion, which was used by the Terasic AD/DA board [8]. The AD/DA panel converts the 14-bit data into an analogue value, therefore, it was necessary to convert the output signals length of the existing PLL structure. This shortening did not influence the analysis of the structure performances. The Altera DE2 board, together with the Terasic AD/DA board, is shown in Fig. 5.

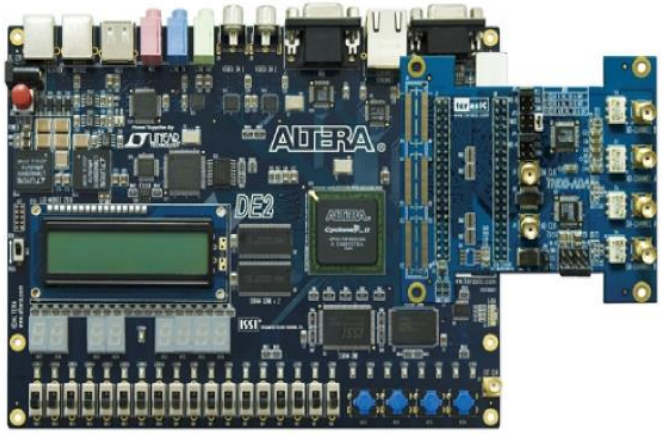

Figure 5. Altera DE2 board with Terasic AD/DA board [8]

Experimental results showing the behavior of a discrete SRF-PLL structure with a DC-SOGI block implemented on the FPGA board and derived from DA converter output are presented in this paper. Simulation results of the discrete SRF-PLL structure obtained in Simulink and ModelSim environment [6] showed that the discrete structure behaves identically as the structure in the continious domain, and deviations are minimized. In these simulations, the structure response for different values of the k_i parameter was tested, in the cases of frequency and amplitude grid voltage step changes, as well as the ability to estimate the grid parameters if DC offset is measured in grid voltage. Simulation results proved the validity of the mathematically derived values of the two-phase generator control loops. The results of the implementation of SRF-PLL structure on the FPGA board are also satisfactory.

First, DC-SOGI block of the discrete SRF-PLL structure is implemented on FPGA board in order to analyze the time of DC offset estimation. As a test signal at the input of the DC-SOGI block, is DC offset step change to 50% of the amplitude grid voltage normalized to one. Fig. 6 shows the time of DC offset estimation at the output of DC-SOGI block control loop, where the block is implemented on FPGA board. The experiment was performed for three different values of the k_i parameter: (10, k_{iopt} = 86.54, 500). From Fig. 6 it can be seen that for lower values of the k_i parameter (k_i=10), the estimation time of DC offset at the control loop output is about 0.5 s, which is too slow and negatively affects the dynamic behavior of the entire SRF-PLL structure. On the other hand, if the value of k_i parameter is large (k_i=500), there are undesired damped oscillations in the estimated value. For the parameter optimum value k_{iopt} =86.54, the transition process ends in 0.1 s, which is in accordance with the performed analysis and with the control loop simulations in the continious and discrete domain.

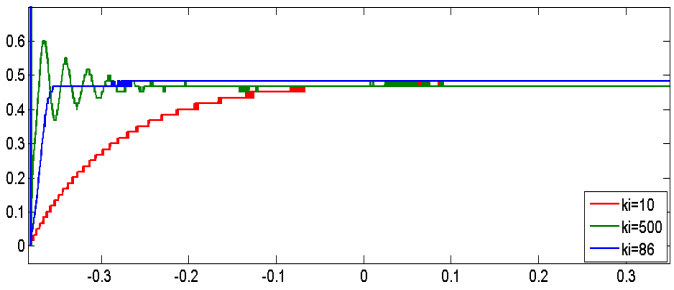

Figure 6. DC offset estimation at the output of DC-SOGI block control loop, with DC offset step change to 50% of grid voltage amplitude normalized to 1

The following analysis refers to the behavior of the SRF-PLL structure with the DC-SOGI block for two cases. In the first case, the grid parameters have reached their stationary states and need to be estimated, and in the second case, time for estimation of grid parameters are analyzed in the case of input voltage step changes. The behavior of the SRF-PLL structure was tested with simulations in Simulink and ModelSim environment [6], followed by the implementation on the FPGA board. For the grid frequency and amplitude estimation in a stationary state, at the structure input is brought sinus signal $v_{in}(t) = sin(\omega t)$, where amplitude is normalized to one, with a small and large percentage of the DC offset (5% and 50% of the normed value). The tests were performed for two frequency limits of 49 Hz and 51 Hz and for two amplitude limit values: 0.5 and 1.35 of the normalized grid voltage values, according to defined international standards such as: IEEE 1547 and IEC 61727. If there is DC offset in measured grid voltage, grid parameters in the stationary state have waves if zhere is no control loop for DC offset elimination. Therefore, in these cases it is impossible to accurately determine the value of these parameters. On the other hand, when a control loop is applied, it completely eliminates the DC offset and there are no waves in the estimated grid parameters. The results are shown in Figs.

7-16. It should be noted that in Figs. 7-10 and Fig. 15 (frequency estimation in stationary state and frequency step change) there is an offset of 0.5 Hz, which is result of data conversion from an oscilloscope into a form acceptable to MATLAB, a program in which graphics were drawn.

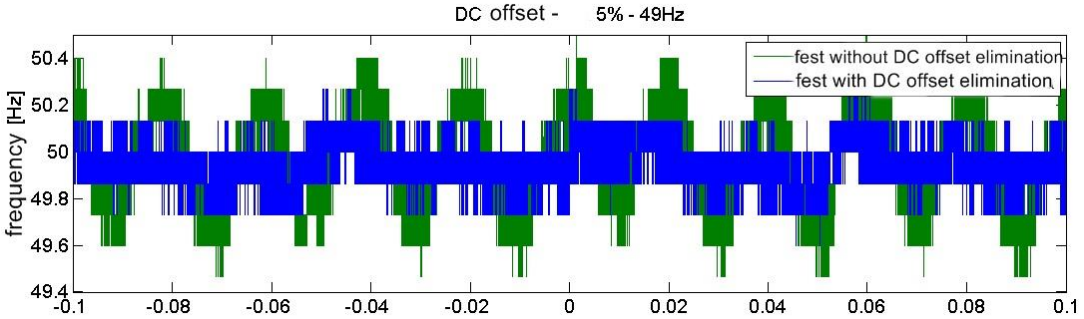

Figure 7. Estimated grid frequency of 49 Hz with 5% DC offset in stationary state without (green line) and with (blue line) control loop for DC offset elimination

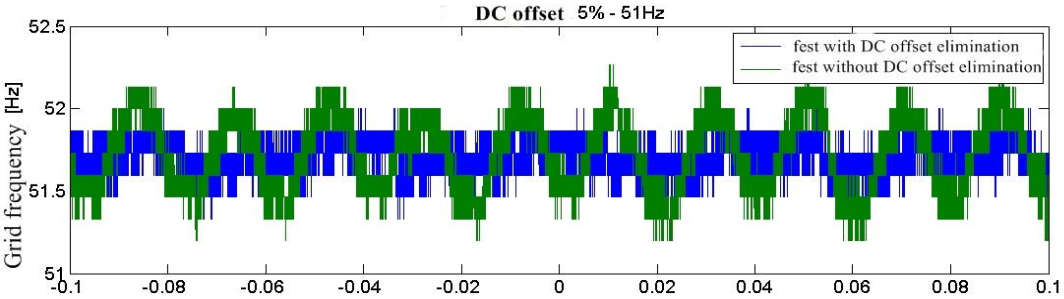

Figure 8. Estimated grid frequency of 51 Hz with 5% DC offset in stationary state without (green line) and with (blue line) control loop for DC offset elimination

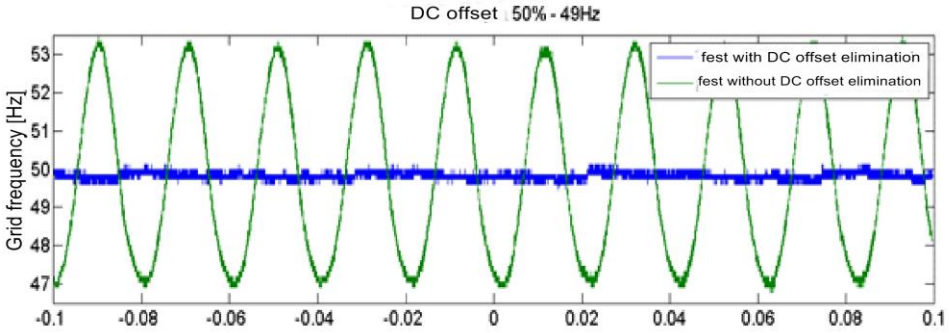

Figure 9. Estimated grid frequency of 49 Hz with 50% DC offset in stationary state without (green line) and with (blue line) control loop for DC offset elimination

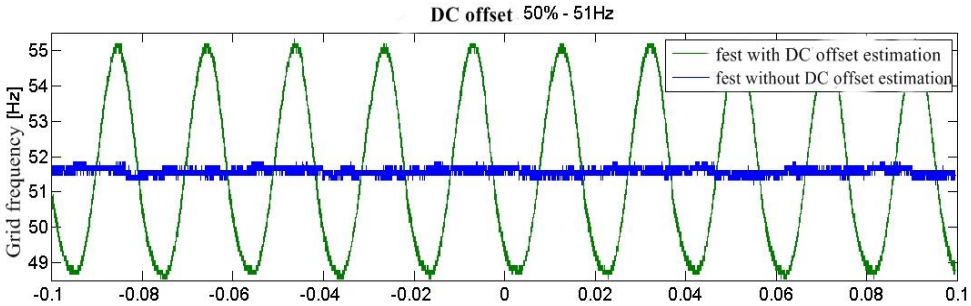

Figure 10. Estimated grid frequency of 51 Hz with 50% DC offset in stationary state without (green line) and with (blue line) control loop for DC offset elimination

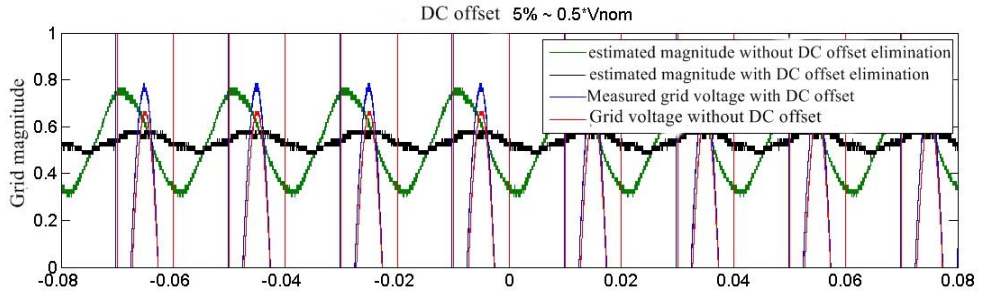

Figure 11. Estimated grid magnitude of 0.5 *V_{nom} with 5% DC offset in stationary state without (green line) and with (black line) control loop for DC offset elimination

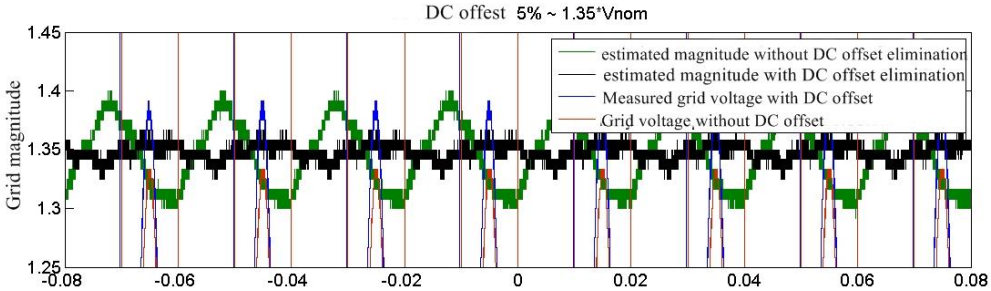

Figure 12. Estimated grid magnitude of 1.35 *V_{nom} with 5% DC offset in stationary state without (green line) and with (black line) control loop for DC offset elimination

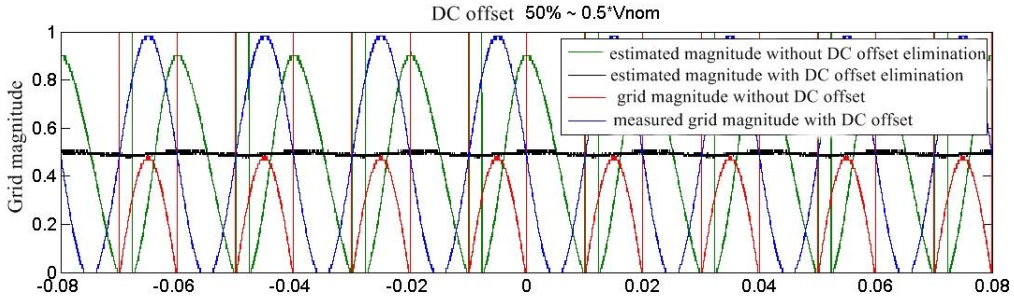

Figure 13. Estimated grid magnitude of 0.5 *V_{nom} with 50% DC offset in stationary state without (green line) and with (black line) control loop for DC offset elimination

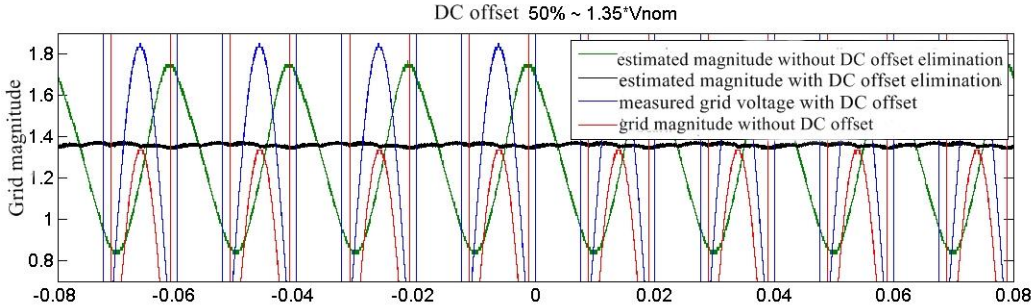

Figure 14. Estimated grid magnitude of 1.35 *V_{nom} with 50% DC offset in stationary state without (green line) and with (black line) control loop for DC offset elimination

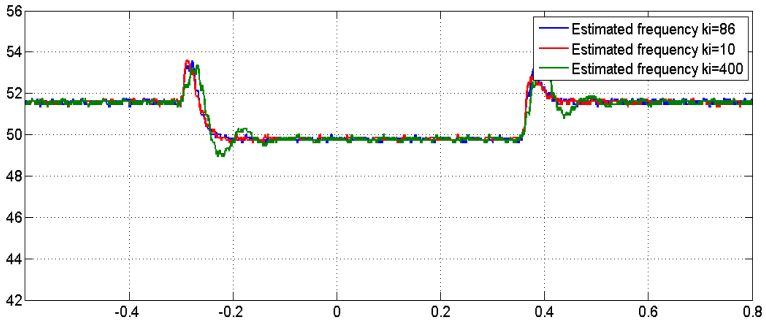

Figure 15. Dinamics of SRF-PLL structure for step change of grid frequency from 51 Hz to 49 Hz and vice versa

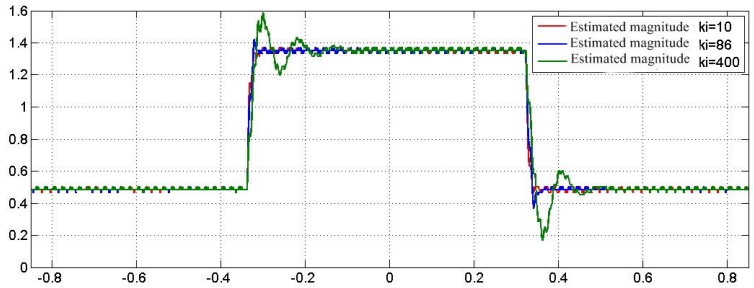

Figure 16. Dinamics of SRF-PLL structure for step change of grid magnitude from 0.5 *V_{nom} to 1.35 *V_{nom} and vice versa

VI. CONCLUSION

In single-phase systems, generating two quadrature signals is much more complicated, since they are derived from a single-phase grid voltage. For this purpose, it is necessary to design a two-phase generator. After analyzing the existing two-phase generators for single-phase PLL structures (SOGI-PLL and Park-PLL), an improved two-phase generator is proposed – DC-SOGI block, which besides generating quadrature signals has the possibility of eliminating the noise and DC offset from grid voltage if they are measured. The performed mathematical analysis showed how to adjust the parameters of this two-phase generator so that the responses of the SRF-PLL structure to the amplitude or frequency jump are optimal. The value of an integral gain of control loop which eliminate DC offset affects both the efficiency of elimination and the speed of grid parameters estimation. To implement SRF-PLL structure on some digital device it was necessary to discretize structure. First, the improved two-phase generator was discretized, and then all other blocks of the SRF-PLL structure. Mathematical analysis showed that the discretization of a two-phase generator does not affect the stability and response of the structure, and then simulations proved this fact. In order for the SRF-PLL structure to be implemented on the FPGA circuit, all the signals of this structure that are presented in the fixed-point format. This conversion usually can significantly affect the operation of the structure unless the appropriate bit length is selected for representing the broken and integer part of the number. For the correctly selected lengths of the broken and integer part deviations are minimal. The blocks of this modified SRF-PLL structure are coded using the Simulink HDL coder, followed by designing digital SRF-PLL structure in the Quartus environment. Simulations of this structure are performed in the ModelSim environment too. Comparing simulation results from Simulink and ModelSim environment, it is concluded that the structure performances even after the coding process remained very good. At the end, structure is implemented on FPGA board, and performances of the structure are presented. Conclusion is the same. Implementation once again confirmed that the structure performances remained very good on digital device.

In the future steps, the proposed two-phase generator should be modified in order to solve problems caused by the appearance of higher harmonics in the grid voltage, and the symmetrical and asymmetric saturation (cutting) of the measured grid voltage.

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